Claims:

1. A quadrature oscillator with phase error correction, comprising:

a local oscillator that generates a single-ended clock signal;

a single-ended to differential converter, coupled to the local oscillator, that converts the single-ended clock signal to a differential clock signal;

a quadrature generator, coupled to the converter, that converts the differential clock signal into an in-phase (I) carrier signal and a quadrature (Q) carrier signal;

a phase error detector, coupled to the quadrature generator, that measures a phase error between the I and Q carrier signals and that provides a phase error signal; and

a feedback amplifier, coupled to the phase error detector and the quadrature generator, that modifies the differential clock signal based on measured phase error.

2. The quadrature oscillator of claim 1, wherein the single-ended to differential converter includes a second stage that generates a pair of differential clock signals.

3. The quadrature oscillator of claim 1, wherein the quadrature generator divides the frequency by two.

4. The quadrature oscillator of claim 1, wherein the feedback amplifier applies the measured phase error as a DC offset to an AC differential clock signal.

5. The quadrature oscillator of claim 1, further comprising:

the local oscillator asserting the single-ended clock signal as a voltage signal;

the single-ended to differential converter asserting the differential clock signal as a differential voltage signal;

a transconductor, coupled to the single-ended to differential converter and the quadrature generator, that converts the differential clock voltage signal into two pairs of differential current clock signals; and

the quadrature generator comprising a master-slave latch configuration, coupled to the transconductor, that generates I and Q current signal outputs from the two pairs of differential current clock signals.

6. The quadrature oscillator of claim 5, wherein the transconductor comprises:

a dual pair of common-emitter coupled transistors, each pair having a base input receiving a component of the differential clock signal and each pair having a pair of collectors generating a corresponding one of the two pairs of differential current clock signals; and

a current source coupled between the emitters of each of the dual pair of transistors and ground.

7. The quadrature oscillator of claim 5, further comprising:

a first chain of buffers that amplifies the I current signal output to provide the I carrier signal; and

a second chain of buffers that amplifies the Q current signal output to provide the Q carrier signal.

8. The quadrature oscillator of claim 7, wherein the phase error detector generates a phase error voltage indicative of phase error between the I and Q carrier signals.

9. The quadrature oscillator of claim 8, wherein the feedback amplifier comprises:

a transconductance stage, coupled to the phase error detector and the quadrature generator, that converts a phase error voltage into a correction current and that adds the correction current to each of the two pairs of differential current clock signals.

10. The quadrature oscillator of claim 9, wherein the transconductance stage comprises MOSFET current sources.

11. The quadrature oscillator of claim 9, wherein the feedback amplifier further comprises:

an RC filter, coupled to the phase error detector; and

an amplifier stage, coupled to the RC filter and the transconductor stage, that amplifies the phase error voltage.

12. The quadrature oscillator of claim 1, wherein the phase error detector comprises:

a first mode buffer, coupled to the quadrature generator, that generates first mode I and Q carrier signals;

a second mode buffer, coupled to the quadrature generator, that generates second mode I and Q carrier signals;

a first phase error detector that measures a phase error between the first mode I and Q carrier signals and that provides a first mode phase error signal;

a second phase error detector that measures a phase error between the second mode I and Q carrier signals and that provides a second mode phase error signal; and

a mode switch, coupled to the first and second phase error detectors and the feedback amplifier, that couples the first phase error detector to the feedback amplifier in a first mode and that couples the second phase error detector to the feedback amplifier in a second mode.

13. A quadrature local oscillator with phase error correction, comprising:

a single-ended to differential converter that converts a single-ended clock signal to a differential clock signal;

a transconductor, coupled to the single-ended to differential converter, that converts the differential clock signal into a pair of differential clock signals;

a quadrature generator, coupled to the transconductor, that converts the pair of differential clock signals into an in-phase (I) clock signal and a quadrature (Q) clock signal;

a first chain of buffers, coupled to the quadrature generator, that develops an I carrier signal as a corrected version of the I clock signal, the first chain of buffers having an intermediate feedback junction;

a second chain of buffers, coupled to the quadrature generator, that develops a Q carrier signal as a corrected version of the Q clock signal, the second chain of buffers having an intermediate feedback junction;

a phase error detector, coupled to the first and second chain of buffers, that measures a phase error between the I and Q carrier signals and that provides a phase error signal;

a feedback amplifier, coupled to the phase error detector, that receives the phase error signal and that generates a differential feedback signal; and

a pair of tuning elements, each coupled to the feedback amplifier and a respective one of the intermediate feedback junctions of the first and second chain of buffers.

14. The quadrature local oscillator of claim 13, wherein each of the pair of tuning elements comprises a tunable RC circuit.

15. The quadrature local oscillator of claim 13, wherein each of the pair of tuning elements comprises:

a series resistance coupled between successive buffers of the chain of buffers; and

a tunable varactor coupled to the resistance and the feedback amplifier.

16. A quadrature oscillator with phase error correction, comprising:

a clock generator that provides a clock signal;

a clock splitter, coupled to the clock generator, that splits the clock signal into first and second clock signals;

a first phase shifting network, coupled to the clock splitter, that develops a first carrier signal based on the first clock signal;

a second phase shifting network, coupled to the clock splitter, that develops a second carrier signal based on the second clock signal, wherein the second clock signal intended to be one quarter phase shifted relative to the first carrier signal; and

a phase detector, coupled to the first and second phase shifting networks, that asserts a phase error signal used to control the phase shifting networks.

17. The quadrature oscillator of claim 16, further comprising:

a combiner, coupled to the phase detector and the clock splitter, that adjusts the first and second clock signals based on the phase error signal.

18. The quadrature oscillator of claim 16, further comprising:

the first and second phase shifting networks each developing a respective one of first and second intermediate carrier signals; and

a combiner, coupled to the phase detector and the first and second phase shifting networks, that adjusts the first and second intermediate carrier signals based on the phase error signal.

19. A method of generating quadrature signals with phase error correction, comprising:

generating a clock signal;

converting the clock signal into a differential clock signal;

splitting the clock signal into first and second clock signals;

developing an in-phase (I) differential carrier signal and a quadrature phase (Q) differential carrier signal based on the first and second clock signals;

detecting phase error between the I and Q differential carrier signals and generating a phase error feedback signal; and

adjusting the phase differential between the I and Q differential carrier signals based on the phase error feedback signal.

20. The method of claim 19, wherein the adjusting the phase differential comprises combining the phase error feedback signal with the first and second clock signals.

21. The method of claim 19, further comprising:

generating intermediate I and Q differential carrier signals within a chain of buffers; and

the adjusting the phase differential comprises combining the phase error feedback signal with the intermediate I and Q differential carrier signals.